CBTL04DP211

DisplayPort 2 : 1 multiplexer

Rev. 2 — 13 April 2012 Product data sheet

1. General description

CBTL04DP211 is an (Embedded) DisplayPort multiplexer for DisplayPort v1.1a switching and multiplexing applications on PC platforms. It is capable of 1 : 2 switching or 2 : 1 multiplexing of 2-lane DisplayPort Main Link signals, using high-bandwidth pass-gate technology. Also, it can switch/multiplex Hot Plug Detect (HPD) signal and AUX signals, for a total of four channels on the display side.

To facilitate DisplayPort switching/multiplexing scheme on PC platforms suitably, CBTL04DP211 provides two separate selection pins (GPU_SEL, AUX_SEL). The selection pin GPU_SEL performs switching from one Main Link to another Main Link. HPD signals will also be switched using the same selection pin. A separate select pin (AUX_SEL) provides additional selection between two AUX channels such that the AUX channel selection is independent of the Main Link and HPD signal selection.

A typical application of CBTL04DP211 is on motherboards where one of two GPU/CPU display sources needs to be selected to connect to a DisplayPort sink device or connector. A controller chip selects which path to use by setting a select signal HIGH or LOW. Due to the non-directional nature of the signal paths (which use high-bandwidth pass-gate technology), the CBTL04DP211 can also be used in the reverse topology, e.g., to connect one DisplayPort source device to one of two DisplayPort sink devices or connectors.

2. Features and benefits

- Supports DisplayPort v1.1a: 1.62 Gbit/s, 2.7 Gbit/s
- Supports Embedded DisplayPort v1.2: 1.62 Gbit/s, 2.7 Gbit/s
- Supports 1-lane, 2-lane Main Link operation
- 1 : 2 switching or 2 : 1 multiplexing of DisplayPort Main Link signals
  - 2 high-speed differential channels with 2 : 1 multiplexing/switching for DisplayPort Main Link signals
  - 1 channel with 2 : 1 multiplexing/switching for AUX signals
  - 1 channel with 2 : 1 multiplexing/switching for single-ended HPD signals
- High-bandwidth analog pass-gate technology
- Very low intra-pair differential skew (5 ps typical)
- Very low inter-pair skew (< 180 ps)
- Switch/multiplexer position select CMOS input
- Single 3.3 V power supply
- Very low operation current of 0.2 mA typical
- ESD 8 kV HBM, 1 kV CDM
- ESD 2 kV HBM, 500 V CDM for control pins
- Available in 3 mm × 6 mm, 0.4 mm pitch HVQFN32 package

3. Applications

- Motherboard applications requiring (embedded) DisplayPort switching/multiplexing
- Docking stations
- Notebook computers
- Chip sets requiring flexible allocation of DisplayPort I/O pins to board connectors

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
CBTL04DP211BS[1]	L04DP211	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 3 × 6 × 0.85 mm[2]	SOT1185-1

[1] Industrial temperature range.

[2] Total height after printed-circuit board mounting = 1 mm (maximum).

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5. Functional diagram

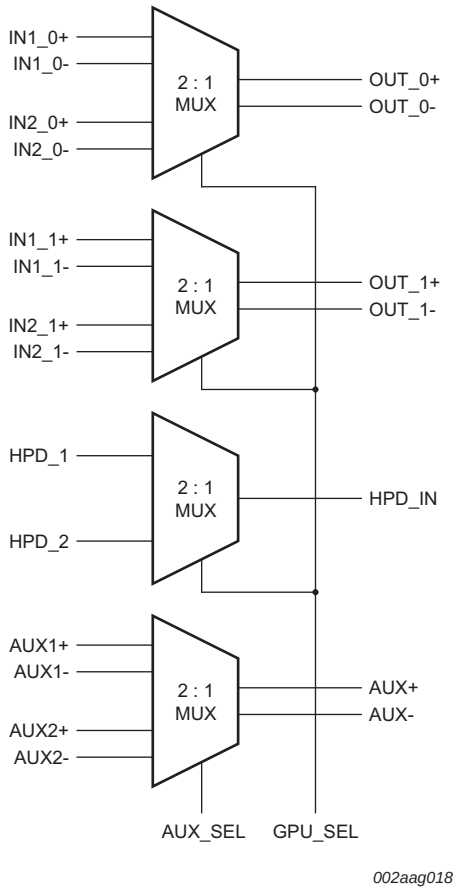

Fig 1. Functional diagram

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6. Pinning information

6.1 Pinning

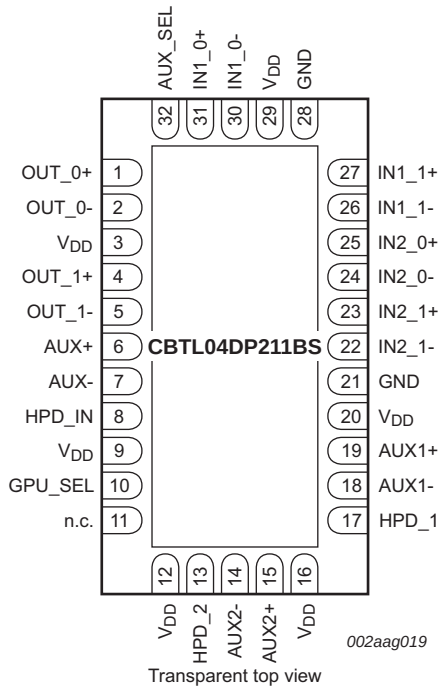

Fig 2. Pin configuration for HVQFN32

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
GPU_SEL	10	3.3 V CMOS single-ended input	Selection for Main Link and Hot Plug Detect signals between two multiplexer/switch paths. When HIGH, path 2 is connected to its corresponding I/O. When LOW, path 1 is connected to its corresponding I/O.
AUX_SEL	32	3.3 V CMOS single-ended input	Selects between AUX paths. When HIGH, AUX2 (path 2) input is connected to AUX output. When LOW, AUX1 (path 1) input is connected to AUX output.
IN1_0+	31	differential I/O	Two bidirectional high-speed differential pairs for DisplayPort Main Link signals, path 1.
IN1_0–	30	differential I/O	
IN1_1+	27	differential I/O	
IN1_1–	26	differential I/O	
IN2_0+	25	differential I/O	Two bidirectional high-speed differential pairs for DisplayPort Main Link signals, path 2.
IN2_0–	24	differential I/O	
IN2_1+	23	differential I/O	
IN2_1–	22	differential I/O	

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Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
OUT_0+	1	differential I/O	Two bidirectional high-speed differential pairs for DisplayPort Main Link signals.
OUT_0–	2	differential I/O	
OUT_1+	4	differential I/O	
OUT_1–	5	differential I/O	
AUX1+	19	differential I/O	High-speed differential pair for AUX signals, path 1.
AUX1–	18	differential I/O	
AUX2+	15	differential I/O	High-speed differential pair for AUX signals, path 2.
AUX2–	14	differential I/O	
AUX+	6	differential I/O	High-speed differential pair for AUX signals.
AUX–	7	differential I/O	
HPD_1	17	single-ended I/O	Single-ended channel for the HPD signal, path 1.
HPD_2	13	single-ended I/O	Single-ended channel for the HPD signal, path 2.
HPD_IN	8	single-ended I/O	Single-ended channel for the HPD signal.
V_{DD}	3, 9, 12, 16, 20, 29	power supply	3.3 V power supply.
GND[1]	21, 28, center pad	ground	Ground.
n.c.	11	-	Not connected. This pin is not connected to any signal internally.

[1] HVQFN32 package die supply ground is connected to both GND pins and exposed center pad. GND pins and the exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

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7. Functional description

Refer to Figure 1 “Functional diagram”.

The CBTL04DP211 uses a 3.3 V power supply. All Main Link signal paths are implemented using high-bandwidth pass-gate technology and are non-directional. No clock or reset signal is needed for the multiplexer to function.

The switch position for the main link differential channels and Hot Plug Detect signals is selected using the select signal GPU_SEL. Additionally, the signal AUX_SEL selects between two AUX positions. The detailed operation is described in Section 7.1 “Multiplexer/switch select functions”.

7.1 Multiplexer/switch select functions

The internal multiplexer switch position is controlled by two logic inputs GPU_SEL and AUX_SEL as described below.

Table 3. Multiplexer/switch select control for IN and OUT channels

GPU_SEL	IN1_n	IN2_n
0	active; connected to OUT_n	high-impedance
1	high-impedance	active; connected to OUT_n

Table 4. Multiplexer/switch select control for HPD channel

GPU_SEL	HPD_1	HPD_2
0	active; connected to HPD_IN	high-impedance
1	high-impedance	active; connected to HPD_IN

Table 5. Multiplexer/switch select control for AUX channels

AUX_SEL	AUX1	AUX2
0	active; connected to AUX	high-impedance
1	high-impedance	active; connected to AUX

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8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.3	+5	V
T_{case}	case temperature			–40	+85	°C
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	8000	V
		HBM; CMOS inputs	[1]	-	2000	V
		CDM	[2]	-	1000	V
		CDM; CMOS inputs	[2]		500	V

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			3.0	3.3	3.6	V
V_I	input voltage	CMOS inputs		–0.3	-	V_{DD} + 0.3	V
		Main Link		–0.3	-	V_{DD} + 0.3	V
		HPD inputs	[1]	–0.3	-	V_{DD} + 0.3	V
		AUX	[2]	–0.3	-	V_{DD} + 0.3	V
T_{amb}	ambient temperature	operating in free air		–40	-	+85	°C

[1] HPD input is tolerant to 5 V input, provided a 1 kΩ series resistor between the voltage source and the pin is placed in series. See Section 11.1 “Special considerations”.

[2] AUX input is tolerant to 5 V input, provided a 2.2 kΩ series resistor between the voltage source and the pin is placed in series. See Section 11.1 “Special considerations”.

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10. Characteristics

10.1 General characteristics

Table 8. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	V_{DD} = 3.3 V	-	200	500	µA
P_{cons}	power consumption	V_{DD} = 3.3 V	-	-	4	mW
$t_{startup}$	start-up time	supply voltage valid to channel specified operating characteristics	-	-	10	µs
t_{rcfg}	reconfiguration time	GPU_SEL or AUX_SEL state change to channel specified operating characteristics	-	-	1	µs

10.2 DisplayPort Main Link channel characteristics

Table 9. DisplayPort Main Link channel characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		–0.3	-	+3.3	V
V_{IC}	common-mode input voltage		0	-	2.0	V
V_{ID}	differential input voltage	peak-to-peak	-	-	+1.2	V
DDIL	differential insertion loss	channel is on; f = 100 MHz	-	–1.6	-	dB
		channel is on; f = 1.5 GHz	-	–2.7	-	dB
		channel is off; 0 Hz ≤ f ≤ 1.5 GHz	-	–35	-	dB
DDRL	differential return loss	channel is on; 0 Hz ≤ f ≤ 1.5 GHz	-	–10	-	dB
DDNEXT	differential near-end crosstalk	adjacent channels are on; 0 Hz ≤ f ≤ 1.5 GHz	-	–40	-	dB
B	bandwidth	–3.0 dB intercept	-	2.0	-	GHz
t_{PD}	propagation delay	from INx_n+/INx_n– port to OUT_n+/OUT_n– port or vice versa	-	100	-	ps
$t_{sk(dif)}$	differential skew time	intra-pair	-	5	-	ps
t_{sk}	skew time	inter-pair	-	-	180	ps

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10.3 AUX ports

Table 10. AUX port characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_I	input voltage			–0.3	-	V_{DD} + 0.3	V
V_O	output voltage	50 Ω load		-	-	V_{DD} + 0.3	V
V_{bias}	bias voltage	AUX		0	-	V_{DD}	V
R_{on}	ON-state resistance	$V_{bias} \leq 2.0$ V		-	15	-	Ω
		2.0 V < V_{bias} < V_{DD}		-	30	-	Ω
V_{ID}	differential input voltage	peak-to-peak		-	-	+1.4	V
t_{PD}	propagation delay	from AUXn port to AUX port or vice versa	[1]	-	100	-	ps

[1] Time from AUX input changing state to AUX output changing state. Includes AUX rise/fall time.

10.4 HPD_IN input, HPD_x outputs

Table 11. HPD input and output characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_I	input voltage			–0.3	-	V_{DD} + 0.3	V
V_O	output voltage			-	-	V_{DD} + 0.3	V
t_{PD}	propagation delay	from HPD_IN to HPD_x or vice versa	[1]	-	100	-	ps

[1] Time from HPD_IN changing state to HPD_x changing state. Includes HPD rise/fall time.

10.5 GPU_SEL and AUX_SEL inputs

Table 12. GPU_SEL and AUX_SEL input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{LI}	input leakage current	V_{DD} = 3.6 V; 0.3 V ≤ V_I ≤ 3.9 V	-	-	10	μA

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11. Application information

11.1 Special considerations

Certain cable or dongle misplug scenarios make it possible for a 5 V input condition to occur on pins AUX+ and AUX–, as well as HPD_IN. When AUX+ and AUX– are connected through a minimum of 2.2 kΩ each, the CBTL04DP211 will sink current but will not be damaged. Similarly, HPD_IN may be connected to 5 V via at least a 1 kΩ resistor. (Correct functional operation to specification is not expected in these scenarios.) The latter also prevents the HPD_OUT output from loading down the system HPD signal when power to the CBTL04DP211 is off.

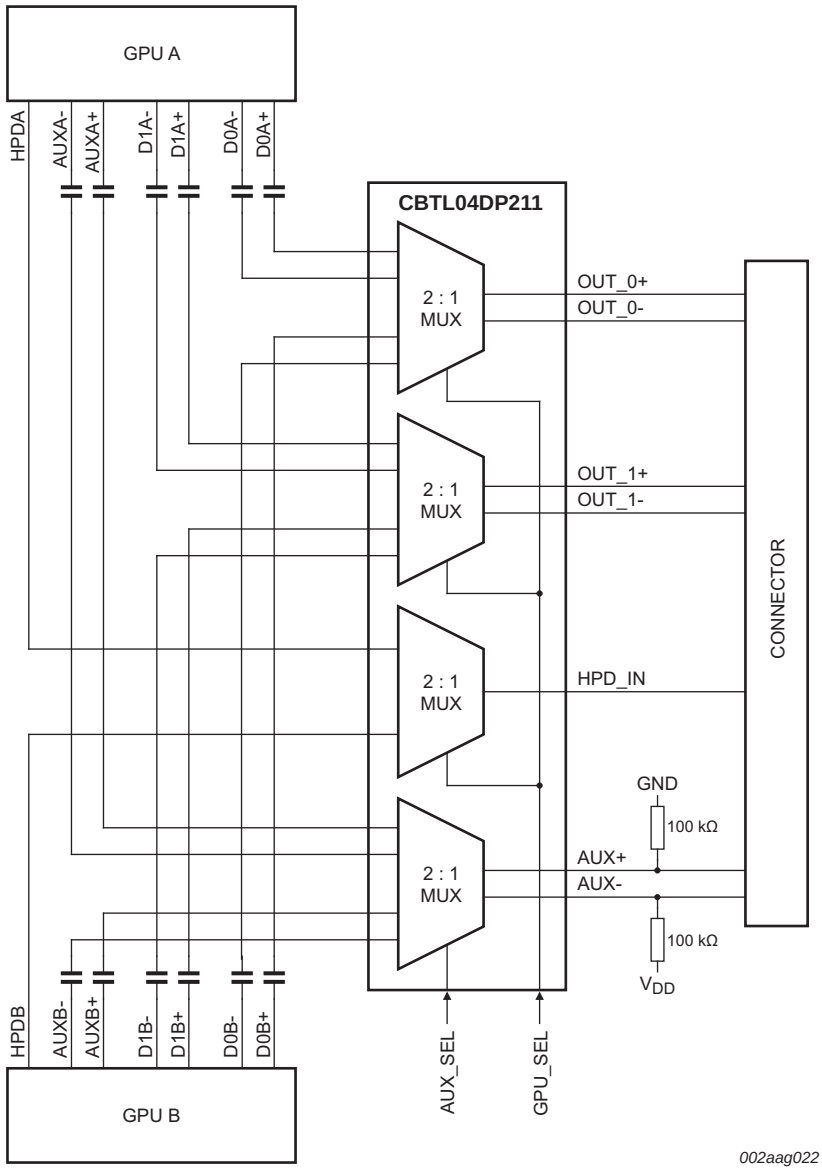

Fig 3. Application diagram

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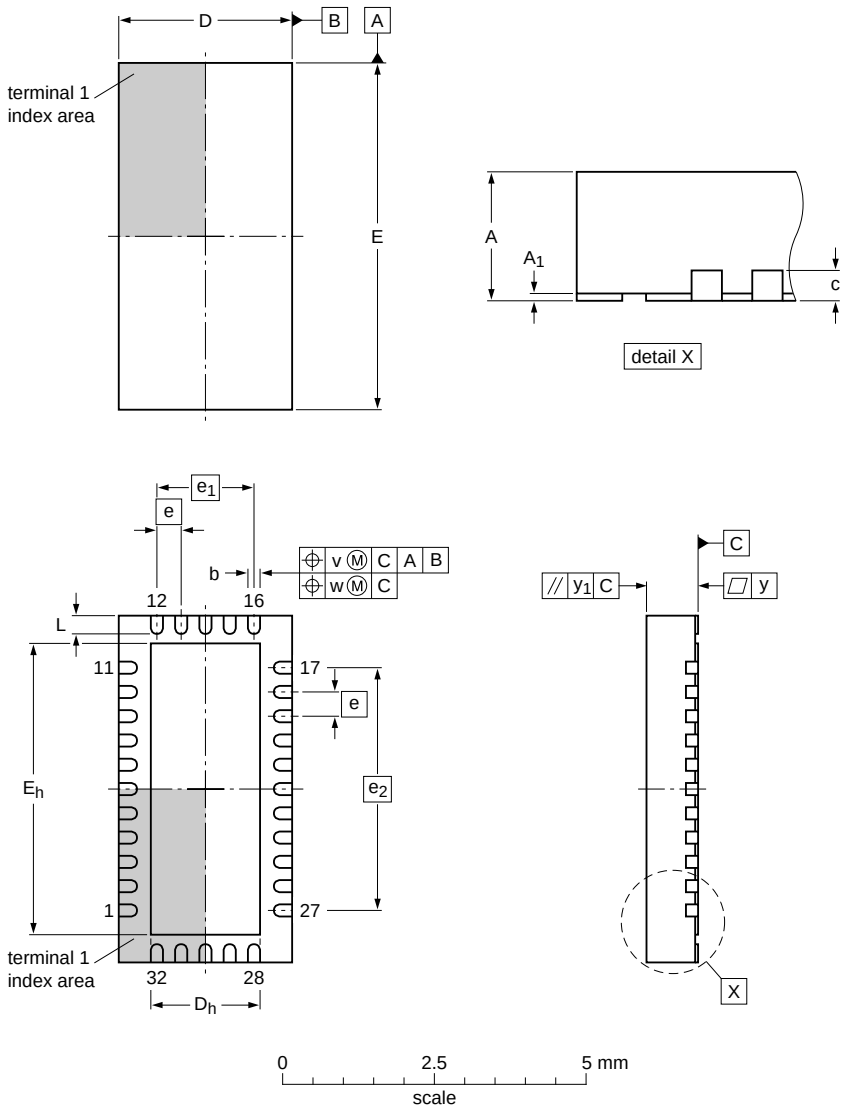
12. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; 3 x 6 x 0.85 mm **SOT1185-1**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.25		3.1	1.9	6.1	4.9				0.4				
	nom	0.85	0.02	0.20	0.2	3.0	1.8	6.0	4.8	0.4	1.6	4	0.3	0.07	0.05	0.08	0.1
	min	0.80	0.00	0.15		2.9	1.7	5.9	4.7				0.2				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1185-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1185-1	- - -	- - -	- - -			~~10-07-26~~ 10-08-09

Fig 4. Package outline SOT1185-1 (HVQFN32)

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13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 5) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 5.

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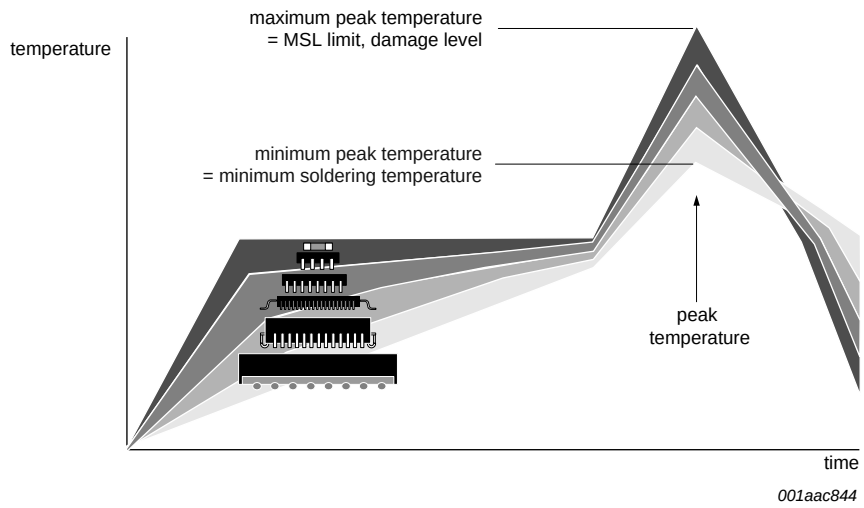

MSL: Moisture Sensitivity Level

Fig 5. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 15. Abbreviations

Acronym	Description
AUX	Auxiliary channel (in DisplayPort definition)
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
ESD	ElectroStatic Discharge
GPU	Graphics Processor Unit
HBM	Human Body Model
HPD	Hot Plug Detect
I/O	Input/Output
PC	Personal Computer

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15. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL04DP211 v.2	20120413	Product data sheet	-	CBTL04DP211 v.1
Modifications:	• Table 1 “Ordering information”: – added “Topside mark” column (Line A marking is corrected from “04DP211” to “L04DP211”) – added (new) Table note [1] • Deleted (old) Section 5 “Marking”			
CBTL04DP211 v.1	20110330	Product data sheet	-	-

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16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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18. Contents

1 General description 1
2 Features and benefits 1
3 Applications 2
4 Ordering information 2
5 Functional diagram 3
6 Pinning information 4
6.1 Pinning 4
6.2 Pin description 4
7 Functional description 6
7.1 Multiplexer/switch select functions 6
8 Limiting values 7
9 Recommended operating conditions 7
10 Characteristics 8
10.1 General characteristics 8
10.2 DisplayPort Main Link channel characteristics . 8
10.3 AUX ports 9
10.4 HPD_IN input, HPD_x outputs 9
10.5 GPU_SEL and AUX_SEL inputs 9
11 Application information 10
11.1 Special considerations 10
12 Package outline 11
13 Soldering of SMD packages 12
13.1 Introduction to soldering 12
13.2 Wave and reflow soldering 12
13.3 Wave soldering 12
13.4 Reflow soldering 13
14 Abbreviations 14
15 Revision history 15
16 Legal information 16
16.1 Data sheet status 16
16.2 Definitions 16
16.3 Disclaimers 16
16.4 Trademarks 17
17 Contact information 17
18 Contents 18

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